

10/050,165  
DOCKET NO. NE253-US

2

**AMENDMENTS TO THE CLAIMS:**

Claim 1. (Previously presented) A semiconductor device comprising:

a plurality of transistors comprising different gate insulator film in their thickness value, said plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said plurality of transistors comprise lightly doped drain regions,

wherein said gate electrode includes an impurity to suppress depletion which is implanted when forming said lightly doped drain regions, and

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

Claim 2. (Previously presented) The semiconductor device according to claim 1, wherein said plurality of transistors comprise a plurality of MOSFETs formed on a substrate.

Claim 3. (Currently amended) The semiconductor according to claim 2,

wherein said plurality of MOSFETs ~~MOSFET~~ includes a core-purpose MOSFET and an I/O-purpose MOSFET, and

wherein said core-purpose MOSFET has a smaller thickness of said gate insulator film than that of said I/O-purpose MOSFET and also has a smaller thickness of said gate electrode than that of said I/O-purpose MOSFET.

Claims 4-6. (Canceled).

10/050,165  
DOCKET NO. NE253-US

3

Claim 7. (Currently amended) The semiconductor device according to claim 1, wherein said plurality of transistors comprise another ~~a first lightly doped drain region and a second~~ lightly doped drain region.

Claim 8. (Currently amended) The semiconductor device according to claim 7, wherein said ~~first~~ lightly doped drain region is deeper than said another ~~second~~ lightly doped drain region.

Claims 9-10. (Canceled).

Claim 11. (Currently amended) The semiconductor device according to claim 2,  
wherein said plurality of MOSFETs ~~MOSFET~~ includes a core-purpose MOSFET and  
an I/O-purpose MOSFET, and  
wherein said core-purpose MOSFET has a smaller thickness of said gate insulator  
film than that of said I/O-purpose MOSFET.

Claim 12. (Currently amended) The semiconductor device according to claim 2,  
wherein said plurality of MOSFETs ~~MOSFET~~ includes a core-purpose MOSFET and  
an I/O-purpose MOSFET, and  
wherein said core-purpose MOSFET has a smaller thickness of said gate electrode  
than that of said I/O-purpose MOSFET.

10/050,165  
DOCKET NO. NE253-US

4

Claim 13. (Previously presented) The semiconductor device according to claim 3, wherein said core-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 1.0v.

Claim 14. (Previously presented) The semiconductor device according to claim 3, wherein said I/O-purpose MOSFET comprises an N - channel MOSFET for being driven on a supply voltage of about 3.3v.

Claim 15. (Currently amended) The semiconductor device according to claim 1, wherein one of said ~~first~~ lightly doped drain regions ~~region~~ comprises an I/O-purpose P-well with an N - type impurity at a predetermined density and a predetermined energy level, wherein said N - type impurity comprises phosphorous.

Claim 16. (Previously presented) The semiconductor device according to claim 15, wherein said predetermined density is about  $2 \times 10^{13}/\text{cm}^2$ , and wherein said predetermined energy level is about 30 keV.

Claim 17. (Currently amended) The semiconductor device according to claim 7, wherein one of said another ~~second~~ lightly doped drain regions ~~region~~ comprises a core-purpose P-well with an N - type impurity implanted at a predetermined density and a predetermined energy level ~~used for implantation~~, wherein said N - type impurity comprises arsenic.

Claim 18. (Previously presented) The semiconductor device according to claim 17,

10/050,165  
DOCKET NO. NE253-US

5

wherein said predetermined density is about  $5 \times 10^{14}/\text{cm}^2$ , and

wherein said predetermined energy level is about 2.5 keV.

Claim 19. (Previously presented) The semiconductor device according to claim 1,  
wherein said plurality of transistors comprise a plurality of sidewalls, said plurality of  
sidewalls comprising a first sidewall and a second sidewall, and  
wherein said first sidewall has a height greater than that of said second sidewall.

Claim 20. (Currently amended) The semiconductor device according to claim 1, wherein  
~~one of said plurality of transistors comprise said~~ lightly doped drain regions comprises region  
with an N - type impurity implanted at a predetermined density and a predetermined energy  
level ~~used for implantation, wherein~~ said N - type impurity comprises arsenic.

Claim 21. (Previously presented) The semiconductor device according to claim 20,  
wherein said predetermined density is about  $5 \times 10^{15}/\text{cm}^2$ , and  
wherein said predetermined energy level is about 30 keV.

Claim 22. (Previously presented) A semiconductor device comprising:  
a plurality of transistors having different gate insulator film thickness values, said  
plurality of types of transistors having different thickness values of a gate electrode thereof in  
correspondence to the thickness values of the gate insulator film thereof,  
wherein said plurality of transistors comprise a plurality of sidewalls, a first lightly  
doped drain region, and a second lightly doped drain region, where said first lightly doped

10/050,165

6

DOCKET NO. NE253-US

drain region and said second lightly doped drain region are formed using said plurality of sidewalls and said gate electrode as a mask, and

wherein said first and second lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.

Claim 23. (Previously presented) A semiconductor device comprising:

a plurality of transistors having different gate insulator film thickness values with a polysilicon film layer, said plurality of transistors having different thickness values of a gate electrode thereof in correspondence to the thickness values of the gate insulator film thereof,

wherein said thickness of said gate insulator film varies based on the amount of deposited gate electrode materials,

wherein said plurality of transistors comprise a plurality of sidewalls, and lightly doped drain regions formed using said plurality of sidewalls and said gate electrode as a mask, and

wherein said lightly doped drain regions have depths corresponding to said thickness values of said gate electrode and said gate insulator film.